What Is Claimed Is:

1. A method for fabricating a semiconductor device comprising:

forming a first gate electrode including a dielectric layer, a first conducting layer, and an insulating layer on a substrate, the first gate electrode functioning as a flash memory;

forming first spacers on sidewalls of the first gate electrode;

forming a second gate electrode comprising a gate oxide layer and a second conducting layer on the substrate, the second gate electrode functioning as a normal gate electrode;

forming a first source/drain region with a shallow junction adjacent to one of the first spacers and a second source/drain region with a shallow junction adjacent to the second gate electrode by performing a first ion implantation process using at least one of the first spacers as a mask;

forming second spacers on a sidewall of the first spacer and on sidewalls of the second gate electrode; and

completing a source/drain region with an LDD region by forming a source/drain region with a deep junction adjacent to the first gate electrode, the source/drain region with the deep junction being formed by a second ion implantation process using the at least one of the second spacers as a mask.

2. A method as defined in claim 1, wherein forming the first spacers comprises:

forming a first insulating layer on the substrate and the first gate electrode; and

performing an etch back process on the first insulating layer.

3. A method as defined in claim 1, wherein forming the second spacers comprises:

forming a second insulating layer on the substrate, the first gate electrode, the first spacers, and the second gate electrode; and

performing an etch back process on the second insulating layer.

4. A semiconductor device comprising:

a first gate electrode and a second gate electrode formed in a single cell on a substrate, the first gate electrode functioning as a flash memory, the second gate electrode functioning as a normal gate electrode;

first spacers formed on sidewalls of the first gate electrode;

second spacers formed on a sidewall of the first spacer and on sidewalls of the second gate electrode; and

a source/drain region with an LDD region formed adjacent to one of the first spacers and adjacent to the second gate electrode.